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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/791,006	03/02/2004	John T. Moore	4305.2US (99-1251.02/US)	1271
24247	7590	12/15/2005	EXAMINER	
TRASK BRITT P.O. BOX 2550 SALT LAKE CITY, UT 84110			TRINH, MICHAEL MANH	
			ART UNIT	PAPER NUMBER
			2822	
DATE MAILED: 12/15/2005				

Please find below and/or attached an Office communication concerning this application or proceeding.

AK

<b>Office Action Summary</b>	<b>Application No.</b>	<b>Applicant(s)</b>	
	10/791,006	MOORE ET AL.	
	<b>Examiner</b>	<b>Art Unit</b>	
	Michael Trinh	2822	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

#### Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

#### Status

- 1) ☒ Responsive to communication(s) filed on 24 October 2005 and 14 November 2005.
- 2a) ☐ This action is **FINAL**.                      2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

#### Disposition of Claims

- 4) ☒ Claim(s) 1-40 is/are pending in the application.
- 4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.
- 5) ☐ Claim(s) \_\_\_\_\_ is/are allowed.
- 6) ☒ Claim(s) 1-40 is/are rejected.
- 7) ☐ Claim(s) \_\_\_\_\_ is/are objected to.
- 8) ☐ Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

#### Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on \_\_\_\_\_ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.  
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

#### Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All    b) ☐ Some \*    c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

\* See the attached detailed Office action for a list of the certified copies not received.

#### Attachment(s)

- |   |   |
|---|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892)             | 4) <input type="checkbox"/> Interview Summary (PTO-413)                     |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948)    | Paper No(s)/Mail Date. _____  |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152) |
| Paper No(s)/Mail Date _____   | 6) <input type="checkbox"/> Other: _____                                    |

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## DETAILED ACTION

\*\*\* This office action is in response to Applicant's amendment and RCE request filed on November 14, 2005. Claims 1-40 are pending.

### *Claim Rejections - 35 USC § 103*

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(f) or (g) prior art under 35 U.S.C. 103(a).

1. Claims 1-40 are rejected under 35 U.S.C. 103(a) as being unpatentable over Aronowitz et al (6,033,998) taken with Mukhopadhyay (6,399,448) and Barsan (5,942,780).

Aronowitz teaches a method for hardening at least a portion of a gate oxide layer on a silicon substrate comprising at least the steps of: forming an oxide layer 206a/206b over the substrate 202; forming a resist layer (Fig 2D) over at least a portion of the oxide layer; patterning the resist layer to create at least at least one exposed area of the oxide layer 206b (Fig 2D; col 5, line 45 through col 7); hardening the at least one exposed area of the oxide layer using a remote plasma nitrogen hardening (RPN) treatment to create at least one hardened area within the oxide layer and at least one non-hardened area within the oxide layer; and thermally growing at least a portion of the at least non-harden area with the oxide layer using a thermal oxidation process to form at least one thick area within the oxide layer (col 6, lines 61-67; Fig 2F), wherein a CMOS device of an integrated circuit including N-channel and P-channel devices (col 2, lines 60-63; lines 8-10). Re further claims 24,4,10,17,30,37,1 wherein, hardening the at least one exposed area of the oxide layer uses a remote plasma nitrogen hardening (RPN) treatment to create at least one hardened area within the oxide layer and at least one non-hardened area (col 6, lines 1-

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50). Re further claims 26,6,12,19,26,32,39, wherein the oxide layer 206 has a thickness of 25 angstroms (col 5, lines 58-65).

Aronowitz lacks patterning a second resist pattern and hardening the second exposed area of the oxide layer, as recited in claim 21 and other independent claims.

However, Mukhopadhyay teaches forming resist layers and patterning to form a first resist pattern 24 (Fig 1) and a second resist pattern 34 (Fig 2) over a portion of the oxide layer to exposed a first area of the oxide layer 12 (Fig 1) and a second area of the oxide layer 12 (Fig 2), and hardening the first exposed area of the oxide layer 12 (Fig 1), and hardening the second exposed area of the oxide layer 12 (Fig 2; col 4, line 8-67), wherein a plurality of areas are exposed and a plurality of thick oxide and thinner oxides 32,42,22 are formed on the substrate (Fig 4; col 5). Barsan teaches forming resist layers and patterning to form a first resist pattern 75 (Fig 4a) and a second resist pattern 4b (Fig 4b; col 8, line 64 through col 9) over a portion of the oxide layer 71 to exposed a first area of the oxide layer (Fig 4a) and a second area of the oxide layer (Fig 4b), and hardening the first exposed area of the oxide layer and hardening the second exposed area of the oxide layer by nitrogen implantation, wherein a plurality of areas are exposed and a plurality of thick oxide and thinner oxides 27,47,55 are formed on the substrate (Fig 4d).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to form the thick and thin oxide layer of Aronowitz by forming a second resist pattern and hardening the second exposed area of the oxide layer, as taught by Mukhopadhyay and Barsan. This is because of the desirability to form an oxide layer having a plurality of first thick oxide, a second thinner oxide layer 42, and a third thinner oxide layer 22 on the semiconductor substrate (Fig 4) so that a plurality of transistors having high voltage and low voltages can be formed on the same substrate at the same time.

Re further claims 5,11,18,25,31,38, Aronowitz teaches (at col 6, lines 5-60) the plasma nitrogen hardening is performed at a temperature of about 60°C (col 6, lines 40-52; and col 7, lines 35-50), a power of 200 W, for a period of time of 120 seconds so as a desired thickness of the oxide layer can be formed. Therefore, the subject matter as a whole would have been obvious to one of ordinary skill in the art at the time the invention was made to select the portion of the prior art's range of parameters, as taught by Aronowitz, and in the semiconductor art, because it has been

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held to be obvious to select a value in a known range by optimization for the best results, and would be an unpatentable modification, where the general conditions of a claim are disclosed in the prior art, it is not inventive to discover the optimum or workable ranges by routine experimentation". *In Re Aller* 104 USPQ 233,255 (CCPA 1955); *In re Waite* 77 USPQ 586 (CCPA 1948); *In Re Swanson* 56 USPQ 372 (CCPA 1942); *In Re Sola* 25 USPQ 433 (CCPA 1935); and *In Re Dreyfus* 24 USPQ 52 (CCPA 1934). Re further claim 35, wherein using these high speed and low power consumption transistors to form a dynamic random access memory device would have been obvious to one of ordinary skill in the art.

### ***Response to Amendment***

\*\* Applicants' remarks in the Amendment submitted October 24, 2005 has avoided the double patenting rejection under 35 U.S.C. 101 of Claims 1-7 and 15-20 over the U.S. Patent No. 6,699,743.

\*\* As already of record, two terminal disclaimers filed on June 13, 2005 disclaiming the terminal portion of any patent granted on this application which would extend beyond the expiration date of U.S. Patent Numbers 6,699,743 and 6,458,663 have been reviewed and accepted. Accordingly, the filing of these terminal disclaimers has also effectively avoided any rejection of obvious-type double patenting rejection of currently pending claims 1-40.

\*\* In view of the Applicant's amendment to the pending claims and in view of the newly cited references of Barsan and Mukhopadhyay, rejection to pending claims 1-40 is applied as above. The indication of allowable of claims 35-40 in the last office action is withdrawn.

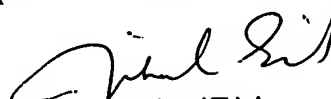
\*\*\*\*\*

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Michael M. Trinh whose telephone number is (571) 272-1847. The examiner can normally be reached on M-F: 8:30 Am to 5:00 Pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Zandra Smith can be reached on (571) 272-2429. The fax phone number is (571) 273-8300.

Any inquiry of a general nature or relating to the status of this application should be directed to the receptionist whose telephone number is (703) 308-0956.

Oacs-1,5,6,102

  
Michael Trinh  
Primary Examiner